REMARKS

This application has been carefully reviewed in light of the Office Action dated June 13, 2005. Applicant has amended claims 1and 8. Reconsideration and favorable action in this case are respectfully requested.

The Examiner has rejected claims 1-5, 7 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 5,906,000 to Abe in view of U.S. Pat. No. 4,818,932 to Odenheimer. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claims 8, 9 and 11 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 4,814,974 to Narayanan in view of U.S. Pat. No. 4,818,932 to Odenheimer and U.S. Pat. No. 5,581,722 to Welland. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 4,814,974 to Narayanan in view of U.S. Pat. No. 4,818,932 to Odenheimer and U.S. Pat. No. 5,581,722 to Welland and further in view of U.S. Pat. No. 5,918,160 to Lysejko. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

Applicant notes with appreciation that the Examiner has indicated that claim 6 would be allowable if rewritten in independent form.

Claims 1 and 8 have been amended for proper antecedent basis. No changes to the substance of the claims has been made.

As noted in the previous Response by Applicant, the Abe reference is directed to a *cache controller* for use with a single CPU. Each entry in the cache memory 18 contains

a tag area and a data area. The tag area (Figure 2) includes a valid/invalid flag 40 for the entry, a priority 42 for the data in the data area and an address indicative of the original location of the data (col. 4, lines 16-21). The priority for an entry is indicative of the frequency of access by the CPU 10 for accessing the data stored in the entry (col. 3, lines 61-64).

A cache memory stores a small subset of a main memory in a high speed memory to allow faster access to data from the main memory that has already been read. As more memory locations are read, some entries in the cache memory will be replaced with data from a different main memory location. The "priority" in the cache memory 18 of Abe is used to determine whether data from a currently read memory location in main memory *will replace the presently stored entry in the cache* (column 5, lines 38-51). The priority described in Abe has nothing whatsoever to do with access to a shared resource and specifically does not prioritize access based on an address space associated with an access request.

The Examiner states that Abe does not explicitly teach a plurality of devices for arbitrating, digital multiple pending requests to the shared resource, with the access priority value assigned to each pending request. The Examiner uses Odenheimer to teach a plurality of devices arbitrating digital, multiple pending requests to the shared resource, with the access priority value assigned to each pending request. The Examiner states that, in Odenheimer, a memory refresh message is given the highest priority and an access request for a message to the digitizer is given the next highest priority.

Abe combined with Odenheimer simply does not teach the present invention. Neither Abe nor Odenheimer teach assigning individual access priority values to a plurality of address space regions. Neither Abe nor Odenheimer teach providing access priority values provided with an access request, such that the access priority value corresponds to an access priority value assigned to an address space region selected by the

target address. Neither Abe nor Odenheimer teach that arbitration between multiple pending requests to the shared resource for access to the shared resource is based at least in part by using the access priority value assigned to each pending request.

These elements of claim 1 define a system where priority on accessing a shared resource is dependent, at least in part, upon the particular regions of address space being accessed in multiple pending requests. This is not a concern in either Abe or Odenheimer, and the Examiner has provided no teaching in Abe or Odenheimer that would even suggest such a manner of arbitration between multiple requests in a shared system. The only "priority" disclosed in Abe is the priority used to determine whether an entry in the cache will be replaced – it has nothing to do with prioritizing multiple access requests. Other than being a multiple processor system, Odenheimer adds nothing to the deficiencies in Abe. The examples of prioritization given by the Examiner, i.e., "a memory refresh message is given the highest priority and an access request for a message to the digitizer is given the next highest priority) again have nothing to do with prioritizing access requests to a shared resource based on what address region in the shared resource is being accessed, as required by the claims. The priority in Odenheimer only specifies priority given to the *type* of message to the shared resource. In Odenheimer, a memory refresh message *to any address* would have priority over any other access. A message to the digitizer would have priority over any access to any address in a shared resource. Odenheimer is explicit that all other requests, i.e., requests to memory, "share least highest priority in alternating fashion." When the digitizer and display interface ports each request access to the same memory bank, the DRAM controller for the bank *alternately* grants memory access to each interface port (col. 9, lines 6-14). Hence, memory access requests are given priority in alternating fashion, *not* based in any manner on the various regions of address space being accessed by the multiple pending requests.

By contrast to the afore-mentioned references, in the present invention defined by claim 1, prioritizing access to a shared resource in a digital system having a plurality of devices vying for access to the shared resource is accomplished by organizing the address space of the shared resource into address space regions and *assigning individual access priority values to a plurality of the address space regions*. An access request specifies a target address within the address space of the shared resource and an access priority value is provided with the access request, *such that the access priority value corresponds to an access priority value assigned to an address space region selected by the target address*. Arbitration between multiple pending requests to the shared resource for access to the shared resource is based at least in part by using the access priority value assigned to each pending request.

Similarly, in independent claim 8, a digital system comprises a shared resource and a plurality of devices connected to access the shared resource. A plurality of memory management units (MMU) are connected to receive an address from a respective one of the plurality of devices, wherein each MMU has storage circuitry for storing a plurality of page entries and each page entry has an access priority field, each MMU being operable to output *an access priority value associated with a received address*. Arbitration circuitry is connected to receive a request signal from each of the plurality of devices and an associated access priority value from each MMU, *wherein the arbitration circuitry is operable to schedule access to the shared resource according to the access priority values*.

As described in connection with the previous response, the other references cited by the Examiner similarly fail to show a prioritization scheme which is based at least in part on the particular region of the address space being accessed by the pending requests. Narayanan teaches a device-based priority scheme where a priority for each device is assigned by a priority designator. Pending access requests to a shared resource are prioritized according to the priority assigned to the particular devices that issued the

requests. Welland is used by the Examiner to show multiple MMUs and does not add any subject matter that would change the prioritization scheme of Narayanan.

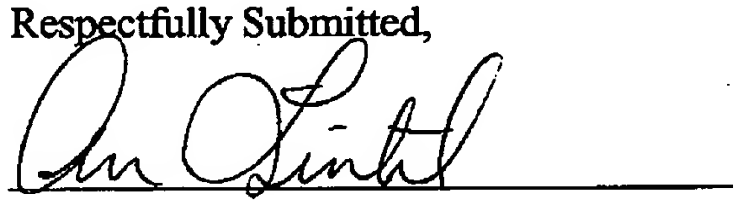
Accordingly, Applicant respectfully requests allowance of claims 1 and 8. Further, Applicant requests allowance of dependent claims 2-7 and 9-12.

The Commissioner is hereby authorized to charge any fees or credit any overpayment, including extension fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Alan W. Lintel, Applicant's Attorney at (972) 664-9595 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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